Atty. Dkt. No.: 39153/447 (G1152)

U.S. PATENT APPLICATION

for

METHOD OF EXTENDING THE AREAS OF CLEAR FIELD PHASE SHIFT GENERATION

Inventors: Todd P. Lukanc
Christopher A. Spence

METHOD OF EXTENDING THE AREAS OF CLEAR FIELD PHASE SHIFT GENERATION

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is related to U.S. Patent Application No. _____, Attorney Docket No. 39153/448 (G1153), entitled METHOD OF ENHANCING CLEAR FIELD PHASE SHIFT MASKS WITH CHROME BORDER AROUND PHASE 180 REGIONS; U.S. Patent Application No. _____, Attorney Docket No. 39153/449 (G1154), entitled METHOD OF ENHANCING CLEAR FIELD PHASE SHIFT MASKS BY ADDING PARALLEL LINE TO PHASE 0 REGION; U.S. Patent Application No. _____, Attorney Docket No. 39153/450 (G1155), entitled METHOD OF ENHANCING CLEAR FIELD PHASE SHIFT MASKS WITH BORDER REGIONS AROUND PHASE 0 AND PHASE 180 REGIONS; and U.S. Patent Application No. _____, Attorney Docket No. 39153/451 (G1156), entitled METHOD OF ENHANCING CLEAR FIELD PHASE SHIFT MASKS WITH BORDER AROUND OUTSIDE EDGES OF PHASE ZERO REGIONS, all of which are assigned to the same assignee as the present application.

[0002] This application is a continuation-in-part (CIP) application claiming priority under 35 U.S.C. 120 to U.S. Patent Application No. _____, filed January 30, 2001, entitled PHASE SHIFT MASK AND SYSTEM AND METHOD FOR MAKING THE SAME, by Todd Lukanc, one of the inventors of the present application.

FIELD OF THE INVENTION

[0003] The present invention relates generally to integrated circuits and methods of manufacturing integrated circuits.

More particularly, the present invention relates to generating phase shifting patterns to improve the patterning of gates and other layers, structures, or regions needing sub-nominal dimensions.

BACKGROUND OF THE INVENTION

[0004] Semiconductor devices or integrated circuits (ICs) can include millions of devices, such as, transistors. Ultra-large scale integrated (ULSI) circuits can include complementary metal oxide semiconductor (CMOS) field effect transistors (FET). Despite the ability of conventional systems and processes to fabricate millions of IC devices on an IC, there is still a need to decrease the size of IC device features, and, thus, increase the number of devices on an IC.

[0005] One limitation to achieving smaller sizes of IC device features is the capability of conventional lithography. Lithography is the process by which a pattern or image is transferred from one medium to another. Conventional IC lithography uses ultra-violet (UV) sensitive photoresist. Ultra-violet light is projected to the photoresist through a reticle or mask to create device patterns on an IC. Conventional IC lithographic processes are limited in their ability to print small features, such as contacts, trenches, polysilicon lines or gate structures.

[0006] Generally, conventional lithographic processes (e.g., projection lithography and EUV lithography) do not have sufficient resolution and accuracy to consistently fabricate small features of minimum size. Resolution can be adversely impacted by a number of phenomena including: diffraction of light, lens aberrations, mechanical stability, contamination, optical properties of resist material, resist contrast, resist swelling, thermal flow of resist, etc. As such, the critical

dimensions of contacts, trenches, gates, and, thus, IC devices, are limited in how small they can be.

[0007] For example, at integrated circuit design feature sizes of 0.5 microns or less, the best resolution for optical lithography technique requires a maximum obtainable numerical aperture (NA) of the lens systems. Superior focus cannot be obtained when good resolution is obtained and vice versa because the depth of field of the lens system is inversely proportional to the NA and the surface of the integrated circuit cannot be optically flat. Consequently, as the minimum realizable dimension is reduced in manufacturing processes for semiconductors, the limits of conventional optical lithography technology are being reached. In particular, as the minimum dimension approaches 0.1 microns, traditional optical lithography techniques may not work effectively.

[0008] With the desire of reducing feature size, integrated circuit (IC) manufacturers established a technique called "phase shifting." In phase shifting, destructive interference caused by two adjacent translucent areas in an optical lithography mask is used to create an unexposed area on the photoresist layer. Phase shifting exploits a phenomenon in which light passing through translucent regions on a mask exhibits a wave characteristic such that the phase of the light exiting from the mask material is a function of the distance the light travels through the mask material. This distance is equal to the thickness of the mask material.

[0009] Phase shifting allows for an enhancement of the quality of the image produced by a mask. A desired unexposed area on the photoresist layer can be produced through the interference of light from adjacent translucent areas having the property that the phase of the light passing through adjacent apertures is shifted by 180 degrees relative

to each other. A dark, unexposed area will be formed on the photoresist layer along the boundary of the phase shifted areas caused by the destructive interference of the light which passes through them.

[0010] Phase shifting masks are well known and have been employed in various configurations as set out by B. J. Lin in the article, "Phase-Shifting Masks Gain an Edge," Circuits and Devices, March 1993, pp. 28-35. The configuration described above has been called alternating phase shift masking (PSM).

[0011] In some cases, phase shifting algorithms employed to design phase shifting masks define a phase shifting area that extends just beyond active regions of an active layer. The remaining length of polysilicon, for example, is typically defined by a field or trim mask. However, this approach is not without its problems. For example, alignment offsets between phase shift masks and field masks may result in kinks or pinched regions in the polysilicon lines as they transition from the phase shifting area to the field mask areas. Also, since the field masks are employed to print the dense, narrow lines of polysilicon beyond the active regions, the field masks become as critical and exacting as the phase shift masks.

[0012] Phase shift patterning of polysilicon or "poly" layouts has been proven to be an enhancement in both manufacturing as well as enabling smaller patterned lines and narrow pitches. These items can be more enhanced as the desired linewidth and pitch shrinks, yet there can be some risks and complications.

[0013] Conventional patterning with phase shifters has been done by shifting only the areas of minimum desired dimensions—

out with similar design rules as that of the patterned poly lines on active regions. As such, there can be many transitions between the phase shifted patterning and binary patterning. Transition areas can result in linewidth loss, increasing device leakage.

[0014] Current alternating phase shift masking (PSM) designs for polysilicon layers often focus on enabling gate shrink by applying alternating phase shift regions around the gate region (i.e., the intersection of the polysilicon and active layers). One such alternating PSM design is described in U.S. Patent No. 5,573,890 entitled METHOD OF OPTICAL LITHOGRAPHY USING PHASE SHIFT MASKING, by Christopher A. Spence (one of the inventors of the present application) and assigned to the assignee of the present application.

[0015] An enhanced phase shift approach was developed to reduce the transition regions and move those regions away from the active edge to wider poly or corners of poly patterns where linewidth loss would have little or no impact. Examples of this enhanced phase shifting approach are described in U.S. Patent Application Serial No. _____, entitled PHASE SHIFT MASK AND SYSTEM AND METHOD FOR MAKING THE SAME, filed on January 30, 2001, by Todd P. Lukanc (one of the inventors of the present application) and assigned to the assignee of the present application, incorporated herein by reference.

[0016] The specification of the Lukanc patent application describes binary and phase masks that define parts of the poly pattern and need to have very controlled critical dimensions (CDs). The phase mask basically has long narrow openings that are easy to pattern but the binary mask has both small openings as well as small lines, in both isolated and dense areas. As such, the patterning of the binary mask can

be complicated and the manufacturing window of this technique can be limited. In both the simple phase and the enhanced phase methods, both masks are critical and have different optimized illumination and patterning conditions.

[0017] Other known systems use a "node" based approach rather than a gate-specific approach to generate a phase assignment that attempts to apply phase shifting to all minimum poly geometries (both field and gate). Two examples of the "node" based approach include, for example, Galan et al. "Applications of Alternating-Type Phase Shift Mask to Polysilicon Level for Random Logic Circuits," Jpn. J. Appl. Phys. Vol. 33 (1994) pp. 6779-6784, Dec. 1994, and U.S. Patent No. 5,807,649 entitled LITHOGRAPHIC PATTERNING METHOD AND MASK SET THEREFOR WITH LIGHT FIELD TRIM MASK, by Liebmann et al.

[0018] In view of the known art, there is a need for improvements to the clear field phase shifting mask (PSM) and field or trim mask approach that result in simpler and more reliable mask fabrication and in better wafer imaging. Further, there is a need to minimize variations or use of optical proximity correction (OPC) by enclosing phase shift masking features. Yet further, there is a need to generate phase shifting patterns to improve the patterning of gates and other layers needing sub-nominal dimensions.

SUMMARY OF THE INVENTION

0019] An exemplary embodiment relates to a method of patterning gates to increase process margins from conventional methods. This technique can be called Full Phase patterning and can define all poly patterns with a phase mask, using only a field or trim mask to resolve

conflicts in the phase mask. The trim mask can expose a series of lines that either separates the different phase areas where patterns are not desired or minimizes the range of sizes of the phase patterns next to a critical gate area.

[0020] An exemplary embodiment of Full Phase pattern generation can be carried out as follows. First the critical poly regions or other region desired to be defined by phase shifting and the poly adjoining are defined. Phase regions are then created on either side of these critical poly regions. These phase regions are assigned phase angles such that regions on either side of the critical poly are 180 degrees out of phase. A next step is to define all remaining poly edges and join as much of these edges to the phase assigned areas as possible. The phase transitions are kept at wide poly areas or at corners or line ends. Next, a boundary around the phase 180 edges not defining the poly edge is defined, and then all area outside that boundary is defined as phase 0. Subnominal lines, spaces, and other violation areas can be cured and optical proximity correction (OPC) can be applied to appropriate areas. Two masks are created. The first is a substantially clear-field phase mask that fully defines the poly pattern and additional artifacts, such as, phase conflicts and phase breaks. The second, a trim mask, is a substantially dark-field mask which removes the phase conflict and phase break regions without impacting the phase-defined poly pattern. The critical patterns on both masks are narrow openings and, thus, have almost identical optimized illumination and patterning conditions.

[0021] Another exemplary embodiment is related to a method of defining a phase shifting mask. This method can include defining critical poly regions and adjoining poly where the critical poly regions are regions desired to be defined by phase shifting, creating phase regions on either side of the critical poly regions, assigning phase angles

to the phase regions such that the phase regions have either a first phase angle or a second phase angle, defining edges of the phase regions being assigned the second phase angle where the edges do not define a poly pattern, defining a boundary region around the defined edges, and defining regions outside a desired poly pattern, phase regions, and boundary region to have the first phase angle. The desired poly pattern, phase regions, and boundary region define a mask.

[0022] Another exemplary embodiment is related to a method of generating phase shifting pattern to improve the patterning of gates and other layers needing sub-nominal dimensions. This method can include defining critical areas, creating phase regions on either side of these critical areas, assigning opposite phase polarities to each side of the critical areas, enhancing the area of the phase regions to reduce patterning errors, defining break regions where phase transitions will be easy to remove later with the trim mask, generating polygons to define other edges and excluding the defined break regions, merging the generated polygons with enhanced critical areas having a common phase polarity, separating the polygons having interactions with more than one polarity into portions which are merged into regions having only one polarity, constructing a boundary region outside of phase 180 regions, and defining undefined regions as phase zero regions.

[0023] Another exemplary embodiment is related to a method of enhancing clear field phase shift masks with a border around outside edges. This method can include assigning phase polarities to the phase regions, defining the edges of the phase regions not defining the poly, establishing a boundary region around these defined edges, and assigning outside of the established boundary to have phase zero.

[0024] Other principle features and advantages of the invention will become apparent to those skilled in the art upon review of the following drawings, the detailed description, and the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] The exemplary embodiments will hereafter be described with reference to the accompanying drawings, wherein like numerals denote like elements, and:

[0026] FIGURE 1 is a flow diagram illustrating steps in a patterning method according to an exemplary embodiment;

[0027] FIGURE 2 is a flow diagram illustrating steps in a patterning method according to another exemplary embodiment;

[0028] FIGURE 3 is a flow diagram illustrating steps in a method of forming a phase shift mask according to an exemplary embodiment;

[0029] FIGURE 4 is a top planar view of a phase shift mask design in accordance with an exemplary embodiment; and

[0030] FIGURE 5 is a top planar view of a field or trim mask design configured for use with the phase shift mask design of FIGURE 4 in accordance with an exemplary embodiment.

DETAILED DESCRIPTION OF THE EXEMPLARY EMBODIMENTS

[0031] FIGURES 1 and 2 provide flow diagrams showing steps in the formation or design of exemplary phase shifting masks. Advantageously, the addition of a boundary region around the entire phase 0 pattern defining polygons improves gate width control, line end

pattern definition, and the manufacturability and patterning process window. This added boundary region balances the "light" on both sides of the line ends resulting in a more predictable final resist pattern. The boundary region also improves the control of the gate width by reducing the coma effect of the stepper. Another advantage is that most of the boundary regions can be merged into long serpentine features that are easier to pattern than small holes.

[0032] FIGURE 1 illustrates a flow diagram 100 of steps in an exemplary method of phase shift mask formation or design. Advantageously, the method increases the process margins from those of conventional methods and systems. The method can include defining all poly patterns with a phase mask and uses the field or trim mask to resolve conflicts in the phase mask. In one embodiment, only the field or trim mask is used to resolve conflicts in the phase mask. The trim mask exposes a series of lines that either separates the different phase areas where patterns are not desired or minimizes the range of sizes of the phase patterns next to a critical gate area.

[0033] In a step 110, phase regions are created on either side of critical poly regions and the poly adjoining these regions either by hand or by a computer algorithm. These defined areas are assigned phase angles (e.g., either 0 or 180 degrees). After step 110, a step 120 is performed in which all remaining poly edges are defined and phase regions are created along as much of these edges as possible without opposite phases touching. The areas of phase transitions are kept at wide poly areas or at corners or line ends. For example, wide poly areas can be defined as 2 times the minimum poly width in thickness.

[0034] In a step 130, a boundary around the phase 180

area outside that boundary is defined as phase 0. After step 140, a step 150 is performed in which now that the mask is basically defined, subnominal lines, spaces, and other violation areas can be cured and optical proximity correction (OPC) can be applied to appropriate areas. The result is a mainly clear phase mask that fully defines the poly pattern leaving only phase conflicts or phase breaks as artifacts and a substantially dark trim mask that cleans up the conflict and boundary areas without impacting the phase defined poly pattern. The critical patterns on both masks are narrow openings and, thus, have almost identical optimized illumination and patterning conditions.

[0035] In yet another exemplary embodiment, the phase 180 regions and boundary regions are defined only around the active gate areas. As such, the phase 180 regions are used to only define the active gate areas and phase 0 defines all other areas. By adding the boundary regions around the phase 180 areas, the mask manufacturing and inspecting are improved.

[0036] Advantageously, a boundary region around the entire phase 0 pattern improves gate width control, line end pattern definition, and the manufacturability and patterning process window. This added boundary region balances the "light" on both sides of the line ends resulting in a more predictable final resist pattern. The boundary region also improves the control of the gate width by reducing the coma effect of the stepper.

[0037] Referring now to FIGURE 2, a flowchart 200

After step 210, a step 220 can be performed in which the areas assigned polarities, or phase definition areas, are enhanced. Enhanced means extended or expanded to include more area.

[0038] In a step 230, break regions are defined for patterns not defined in step 220 for which phase transitions are likely to occur. For example, phase transitions can occur at line ends, at corners or at wide lines regions. Such break locations are regions having a width such that they can be patterned and inspected. After a step 230, a step 240 can be performed in which polygons are generated to define all other edges (e.g., field edges) of the pattern that are not defined in steps 220 and 230.

[0039] After step 240, a step 250 can be performed in which polygon regions from step 240 that interact with only one phase polarity (either phase 0 or phase 180) are merged with polygons of step 220 with the same polarity.

[0040] After step 250, a step 260 is performed in which polygons from step 240 that interact with both polarities of phase defined in step 220 are broken or separated such that the portions can be merged with only one polarity.

[0041] In a step 270, a boundary region is constructed outside of phase 180 polarity regions from step 260 and a boundary region outside the phase 0 polygons regions of step 260. The width of the boundary region is preferably similar to the widths of step 230. The boundary regions and break regions are preferably merged where possible to make patterning easier.

[0042] In a step 280, regions not defined as a desired final pattern, phase 180 polygons, phase 180 border regions, or break regions

are defined as phase 0 regions. In a step 290, clean up steps are performed to "cure" design rule violations or areas that would create mask generation issues. In a step 295, optical proximity and process corrections are applied to the phase regions to allow proper pattern generation.

[0043] In a step 298, a trim mask is generated to remove undesired patterns between the phase 0 and phase 180 regions of the phase mask outside of the desired final pattern. This generation is done by oversizing the boundary and break regions.

[0044] Advantageously, the process described with reference to the FIGURES 1-2 improves gate width control, line end pattern definitions, and the patterning process window. Further, the process can minimize the number of transition regions where bridging or pinching is possible. Moreover, the process can make the critical piece of the trim mask similar to that of the phase mask, namely a relatively narrow opening in the chrome mask (or a trench). Making the critical piece of trim mask similar to the phase mask has an advantage of making the optimized illumination conditions of the phase mask more similar to or the same as the trim mask. By doing this, the stepper does not have to change settings (e.g., numerical aperture or partial coherence or focus or exposure dose).

[0045] FIGURE 3 illustrates a flow diagram 300 depicting exemplary steps in the formation or design of a phase shifting mask (PSM) and a field or trim mask. A set of previously defined phase 0 or phase 180 regions on a phase mask identifies a critical poly section. These phase 0 or phase 180 regions can be created by hand drawing, by using a currently available software program, or by creating an optimized program to define the regions. In exemplary embodiments, the phase 0 or

phase 180 regions are formed or designed in a process, such as, the processes described with reference to FIGURE 1 or FIGURE 2.

[0046] In a step 310, a chrome boundary region is formed on the phase mask outside phase 180 region edges of the previously defined phase 180 regions that are not defining a final poly pattern. This chrome boundary region can be defined by either hand drawing or by using a computer software program. Advantageously, this chrome boundary region makes it easy to inspect the mask, and easy to pattern the phase etch step of making the mask. In a step 320, all regions not defined (either as the final poly pattern or phase 180 regions or chrome boundary regions) are defined as phase 0.

[0047] In a step 330, the chrome is patterned and etched on the mask. As part of the chrome defining process or after the chrome is patterned, a layer of resist is coated and sections of the resist are selectively removed in areas where phase 180 sections are to be formed. In an exemplary embodiment, an oversized phase 180 pattern, or a phase etch region, is defined to allow the resist to be removed and the quartz to be etched. This oversized resist pattern covers any openings in the chrome where it is desired to avoid etching. A dry or wet etch can be used to etch the quartz to a lesser thickness in the formation of the phase 180 regions. The formation of phase 180 sections and phase etch regions are further described with reference to FIGURE 4.

[0048] In a step 340, the trim mask is formed to have openings that are oversized versions of the boundary chrome regions outside the final poly pattern. The openings of the trim mask are oversized because their size is slightly larger in area than the boundary

placed over these slightly smaller boundary regions. An exemplary trim mask is described with reference to FIGURE 5.

[0049] FIGURE 4 illustrates a plan view of a phase mask 400 formed or designed utilizing the process described with reference to FIGURE 3. Phase mask 400 includes poly regions 410, phase 180 regions 420, and phase 0 regions 430. Poly regions 410 (depicted in FIGURE 4 as dotted areas) are critical poly sections. Phase 180 regions 420 and phase 0 regions 430 help to define poly regions 410 and can be created by hand or using a computer software program configured for the designing of phase masks. Phase mask 400 also can include a region 450 outside of defined areas. In an exemplary embodiment, region 450 (depicted in FIGURE 4 as a gray back-hashed area) is assigned a phase of zero.

[0050] Phase etch regions 460 (depicted in FIGURE 2 using a bold dashed line) are areas that define a pattern used in the formation of phase 180 regions 420. Advantageously, the positions of phase etch regions 460 are self-aligned to the chrome pattern as to avoid misplacement of the etch pattern relative to the original chrome pattern. In an alternative embodiment, it is possible to make the etch profile such that it partially goes underneath the chrome to partially hide the etch profile. The partially hidden etch profile allows for some variation in sidewall profiles.

[0051] Trim mask openings 470 (depicted in FIGURE 4 using a dotted line) define an area that is exposed when the field or trim mask is applied. An exemplary trim mask corresponding to trim mask openings 470 is described with reference to FIGURE 5. Trim mask openings 470 are configured to cover interfaces between phase 180 regions and phase 0 regions and correct for artifacts. For example, phase

180 regions 420 and phase 0 region 450 are adjacent to each other at several places on phase mask 400 and artifacts can be created at the locations. Advantageously, trim mask openings 470 help to correct for such artifacts.

[0052] FIGURE 5 illustrates a plan view of a field or trim mask 500. Trim mask 500 is configured for use with phase mask 400 described with reference to FIGURE 4. Trim mask 500 includes openings 510 corresponding to trim mask opening 470 in FIGURE 4.

[0053] While the exemplary embodiments illustrated in the FIGURES and described above are presently preferred, it should be understood that these embodiments are offered by way of example only. Other embodiments may include, for example, different techniques for creating phase shifting regions. The invention is not limited to a particular embodiment, but extends to various modifications, combinations, and permutations that nevertheless fall within the scope and spirit of the appended claims.